The Simple Art Of Soc Design Closing The Gap Between Rtl And Esl

The Simple Art of SoC Design Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers *A Practical Approach to VLSI System on Chip (SoC) Design* **Essential Issues in SOC Design Co-verification of Hardware and Software for ARM SoC Design Engineering the Complex SOC The Simple Art of SoC Design Computer System Design System-on-Chip Design with Arm® Cortex®-M Processors UML for SOC Design** *System on Chip Interfaces for Low Power Design* **Interconnect-Centric Design for Advanced SOC and NOC Low-Power NoC for High-Performance SoC Design Winning the SoC Revolution** Surviving the SOC Revolution **On-Chip Communication Architectures** Modern System-on-Chip Design on Arm Designing SOCs with Configured Cores Advanced HDL Synthesis and SOC Prototyping *Introduction to Advanced System-on-Chip Test Design and Optimization* **Software Architect's Handbook Hardware Software Co-Design of a Multimedia SOC Platform ASIC/SoC Functional Design Verification** Clock Generators for SOC Processors VLSI-Soc *Fundamentals of IP and SoC Security* **VLSI-SoC: Design Trends VLSI-SoC: Design Methodologies for SoC and SiP Essential Issues in SOC Design** Embedded System Design System-on-a-chip Low Power Methodology Manual *System-on-a-Chip Verification* SoC Physical Design **System-on-Chip Security** Modeling Embedded Systems and SoC's Engineering the Complex SOC. **Arm System-On-Chip Architecture, 2/E** *Noise Coupling in System-on-Chip Multiprocessor Systems-on-Chips*

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The Simple Art of SoC Design Oct 29 2022 This book tackles head-on the challenges of digital design in the era of billion-transistor SoCs. It discusses fundamental design concepts in design and coding required to produce robust, functionally correct designs. It also provides specific techniques for measuring and minimizing complexity in RTL code. Finally, it discusses the tradeoff between RTL and high-level (C-based) design and how tools and languages must progress to address the needs of tomorrow's SoC designs.
Designing SOCs with Configured Cores May 12 2021 Microprocessor cores used for SOC design are the direct descendents of Intel's original 4004 microprocessor. Just as packaged microprocessor ICs vary widely in their attributes, so do microprocessors packaged as IP cores. However, SOC designers still compare and select processor cores the way they previously compared and selected packaged microprocessor ICs. The big problem with this selection method is that it assumes that the laws of the microprocessor universe have remained unchanged for decades. This assumption is no longer valid. Processor cores for SOC designs can be far more plastic than microprocessor ICs for board-level system designs. Shaping these cores for specific applications produces much better processor efficiency and much lower system clock rates. Together, Tensilica's Xtensa and Diamond processor cores constitute a family of software-compatible microprocessors covering an extremely wide performance range from simple control processors, to DSPs, to 3-way superscalar processors. Yet all of these processors use the same software-development tools so that programmers familiar with one processor in the family can easily switch to another. This book emphasizes a processor-centric MPSOC (multiple-processor SOC) design style shaped by the realities of the 21st-century and nanometer silicon. It advocates the assignment of tasks to firmware-controlled processors whenever possible to maximize SOC flexibility, cut power dissipation, reduce the size and number of hand-built logic blocks, shrink the associated verification effort, and minimize the overall design risk. · An essential, no-nonsense guide to the design of 21st-century mega-gate SOCs using nanometer silicon. · Discusses today's key issues affecting SOC design, based on author's decades of personal experience in developing large digital systems as a design engineer while working at Hewlett-Packard's Desktop Computer Division and at EDA workstation pioneer Cadnetix, and covering such topics as an award-winning technology journalist and editor-in-chief for EDN magazine and the Microprocessor Report. · Explores conventionally accepted boundaries and perceived limits of processor-based system design and then explodes these artificial constraints through a fresh outlook on and discussion of the special abilities of processor cores designed specifically for SOC design. · Thorough exploration of the evolution of processors and processor cores used for ASIC and SOC design with a look at where the industry has come from, and where it's going. · Easy-to-understand explanations of the capabilities of configurable and extensible processor cores through a detailed examination of Tensilica's configurable, extensible Xtensa processor core and six pre-configured Diamond cores. · The most comprehensive assessment available of the practical aspects of configuring and using multiple processor cores to achieve very difficult and ambitious SOC price, performance, and power design goals.
Engineering the Complex SOC May 24 2022 Engineering the Complex SOC The first unified hardware/software guide to processor-centric SOC design Processor-centric approaches enable SOC designers to complete far larger projects in far less time. Engineering the Complex SOCis a comprehensive, example-driven guide to creating designs with configurable, extensible processors. Drawing upon Tensilica's Xtensa architecture and TIE language, Dr. Chris Rowen systematically illuminates the issues, opportunities, and challenges of processor-centric design. Rowen introduces a radically new design methodology, then covers its essential techniques: processor configuration, extension, hardware/software co-generation, multiple processor partitioning/communication, and more. Coverage includes: Why extensible processors are necessary: shortcomings of current design methods Comparing extensible processors to traditional processors and hardwired logic Extensible processor architecture and mechanisms of processor extensibility Latency, throughput, coordination of parallel functions, hardware interconnect options, management of design complexity, and other issues Multiple-processor SOC architecture for embedded systems Task design from the viewpoints of software andhardware developers Advanced techniques: implementing complex state machines, task-to-task synchronization, power optimization, and more Toward a "sea of processors": Long-term trends in SOC design and semiconductor technology For all architects, hardware engineers, software designers, and SOC program managers involved with complex SOC design; and for all managers investing in SOC designs, platforms, processors, or expertise. PRENTICE HALL Professional Technical Reference Upper Saddle River, NJ 07458 www.phptr.com
Engineering the Complex SOC. Sep 23 2019 *Noise Coupling in System-on-Chip* Jul 22 2019 Noise Coupling is the root-cause of the majority of Systems on Chip (SoC) product fails. The book discusses a breakthrough substrate coupling analysis flow and modelling toolset, addressing the needs of the design community. The flow provides capability to analyze noise components, propagating through the substrate, the parasitic interconnects and the package. Using this book, the reader can analyze and avoid complex noise coupling that degrades RF and mixed signal design performance, while reducing the need for conservative design practices. With chapters written by leading international experts in the field, novel methodologies are provided to identify noise coupling in silicon. It additionally features case studies that can be found in any modern CMOS SoC product for mobile communications, automotive applications and readout front ends.
Low Power Methodology Manual Feb 27 2020 This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low

power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.
Introduction to Advanced System-on-Chip Test Design and Optimization Mar 10 2021 Testing of Integrated Circuits is important to ensure the production of fault-free chips. However, testing is becoming cumbersome and expensive due to the increasing complexity of these ICs. Technology development has made it possible to produce chips where a complete system, with an enormous transistor count, operating at a high clock frequency, is placed on a single die - SOC (System-on-Chip). The device size miniaturization leads to new fault types, the increasing clock frequencies enforces testing for timing faults, and the increasing transistor count results in a higher number of possible fault sites. Testing must handle all these new challenges in an efficient manner having a global system perspective. Test design is applied to make a system testable. In a modular core-based environment where blocks of reusable logic, the so called cores, are integrated to a system, test design for each core include: test method selection, test data (stimuli and responses) generation (ATPG), definition of test data storage and partitioning [off-chip as ATE (Automatic Test Equipment) and/or on-chip as BIST (Built-In Self-Test)], wrapper selection and design (IEEE std 1500), TAM (test access mechanism) design, and test scheduling minimizing a cost function whilst considering limitations and constraint. A system test design perspective that takes all the issues above into account is required in order to develop a globally optimized solution. SOC test design and its optimization is the topic of this book. It gives an introduction to testing, describes the problems related to SOC testing, discusses the modeling granularity and the implementation into EDA (electronic design automation) tools. The book is divided into three sections: i) test concepts, ii) SOC design for test, and iii) SOC test applications. The first part covers an introduction into test problems including faults, fault types, design-flow, design-for-test techniques such as scan-testing and Boundary Scan. The second part of the book discusses SOC related problems such as system modeling, test conflicts, power consumption, test access mechanism design, test scheduling and defect-oriented scheduling. Finally, the third part focuses on SOC applications, such as integrated test scheduling and TAM design, defect-oriented scheduling, and integrating test design with the core selection process.
UML for SOC Design Jan 20 2022 A tutorial approach to using the UML modeling language in system-on-chip design Based on the DAC 2004 tutorial, applicable for students and professionals Contributions by top-level international researchers The best work at the first UML for SoC workshop Unique combination of both UML capabilities and SoC design issues Condenses research and development ideas that are only found in multiple conference proceedings and many other books into one place Will be the seminal reference work for this area for years to come
Essential Issues in SOC Design Jun 01 2020 This book originated from a workshop held at the DATE 2005 conference, namely Designing Complex SOCs. State-of-the-art in issues related to System-on-Chip (SoC) design by leading experts in the fields, it covers IP development, verification, integration, chip implementation, testing and software. It contains valuable academic and industrial examples for those involved with the design of complex SOCs.
Surviving the SOC Revolution Aug 15 2021 From the reviews: "This book crystallizes what may become a defining moment in the electronics industry - the shift to platform-based design. It provides the first comprehensive guidebook for those who will build, and use, the integration platforms that may soon drive the system-on-chip revolution." Electronic Engineering Times
Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers Sep 28 2022 This textbook aims to provide learners with an understanding of embedded systems built around Arm Cortex-M processor cores, a popular CPU architecture often used in modern low-power SoCs that target IoT applications. Readers will be introduced to the basic principles of an embedded system from a high-level hardware and software perspective and will then be taken through the fundamentals of microcontroller architectures and SoC-based designs. Along the way, key topics such as chip design, the features and benefits of Arm's Cortex-M processor architectures (including TrustZone, CMSIS and AMBA), interconnects, peripherals and memory management are discussed. The material covered in this book can be considered as key background for any student intending to major in computer engineering and is suitable for use in an undergraduate course on digital design.
VLSI-SoC: Design Trends Aug 03 2020 This book contains extended and revised versions of the best papers presented at the 28th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2020, held in Salt Lake City, UT, USA, in October 2020.* The 16 full papers included in this volume were carefully reviewed and selected from the 38 papers (out of 74 submissions) presented at the conference. The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of nano-scale, state-of-the-art and emerging manufacturing technologies. In particular they address cutting-edge research fields like low-power design of RF, analog and mixed-signal circuits, EDA tools for the synthesis and verification of heterogenous SoCs, accelerators for cryptography and deep learning and on-chip Interconnection system, reliability and testing, and integration of 3D-ICs. *The conference was held virtually.
SoC Physical Design Dec 27 2019 SoC Physical Design is a comprehensive practical guide for VLSI designers that thoroughly examines and explains the practical physical design flow of system on chip (SoC). The book covers the rationale behind making design decisions on power, performance, and area (PPA) goals for SoC and explains the required design environment algorithms, design flows, constraints, handoff procedures, and design infrastructure requirements in achieving them. The book reveals challenges likely to be faced at each design process and ways to address them in practical design environments. Advanced topics on 3D ICs, EDA trends, and SOC trends are discussed in later chapters. Coverage also includes advanced physical design techniques followed for deep submicron SOC designs. The book provides aspiring VLSI designers, practicing design engineers, and electrical engineering students with a solid background on the complex physical design requirements of SoCs which are required to contribute effectively in design roles.
Modeling Embedded Systems and SoC's Oct 25 2019 System level design is a critical component for the methods to develop designs more productively. But there are a number of challenges in implementing system level modeling. This book addresses that need by developing organizing principles for understanding, assessing, and comparing the different models of computation in system level modeling.
Clock Generators for SOC Processors Nov 06 2020 This book examines the issue of design of fully-integrated frequency synthesizers suitable for system-on-a-chip (SOC) processors. This book takes a more global design perspective in jointly examining the design space at the circuit level as well as at the architectural level. The coverage of the book is comprehensive and includes summary chapters on circuit theory as well as feedback control theory relevant to the operation of phase locked loops (PLLs). On the circuit level, the discussion includes low-voltage analog design in deep submicron digital CMOS processes, effects of supply noise, substrate noise, as well device noise. On the architectural level, the discussion includes PLL analysis using continuous-time as well as discrete-time models, linear and nonlinear effects of PLL performance, and detailed analysis of locking behavior. The material then develops into detailed circuit and architectural analysis of specific clock generation blocks. This includes circuits and architectures of PLLs with high power supply noise immunity and digital PLL architectures where the loop filter is digitized. Methods of generating low-spurious sampling clocks for discrete-time analog blocks are then examined. This includes sigma-delta fractional-N PLLs, Direct Digital Synthesis (DDS) techniques and non-conventional uses of PLLs. Design for test (DFT) issues as they arise in PLLs are then discussed. This includes methods of accurately measuring jitter and built-in-self-test (BIST) techniques for PLLs. Finally, clocking issues commonly associated to system-on-a-chip (SOC) designs, such as multiple clock domain interfacing and partitioning, and accurate clock phase generation techniques using delay-locked loops (DLLs) are also addressed. The book provides numerous real world applications, as well as practical rules-of-thumb for modern designers to use at the system, architectural, as well as the circuit level. This book is well suited for practitioners as well as graduate level students who wish to learn more about time-domain analysis and design of frequency synthesis techniques.
Modern System-on-Chip Design on Arm Jun 13 2021 SoC design has seen significant advances in the decade and Arm-based silicon has often

been at the heart of this revolution. Today, entire systems including processors, memories, sensors and analogue circuitry are all integrated into one single chip (hence "System-on-Chip" or SoC). The aim of this textbook is to expose aspiring and practising SoC designers to the fundamentals and latest developments in SoC design and technologies using examples of Arm(R) Cortex(R)-A technology and related IP blocks and interfaces. The entire SoC design process is discussed in detail, from memory and interconnects through to validation, fabrication and production. A particular highlight of this textbook is the focus on energy efficient SoC design, and the extensive supplementary materials which include a SystemC model of a Zynq chip. This textbook is aimed at final year undergraduate students, master students or engineers in the field looking to update their knowledge. It is assumed that readers will have a pre-existing understanding of RTL, Assembly Language and Operating Systems. For those readers looking for a entry-level introduction to SoC design, we recommend our Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers textbook.

Winning the SoC Revolution Sep 16 2021 In 1998-99, at the dawn of the SoC Revolution, we wrote Surviving the SOC Revolution: A Guide to Platform Based Design. In that book, we focused on presenting guidelines and best practices to aid engineers beginning to design complex System-on-Chip devices (SoCs). Now, in 2003, facing the mid-point of that revolution, we believe that it is time to focus on winning. In this book, Winning the SoC Revolution: Experiences in Real Design, we gather the best practical experiences in how to design SoCs from the most advanced design groups, while setting the issues and techniques in the context of SoC design methodologies. As an edited volume, this book has contributions from the leading design houses who are winning in SoCs - Altera, ARM, IBM, Philips, TI, UC Berkeley, and Xilinx. These chapters present the many facets of SoC design - the platform based approach, how to best utilize IP, Verification, FPGA fabrics as an alternative to ASICs, and next generation process technology issues. We also include observations from Ron Wilson of CMP Media on best practices for SoC design team collaboration. We hope that by utilizing this book, you too, will win the SoC Revolution.

Multiprocessor Systems-on-Chips Jun 20 2019 Modern system-on-chip (SoC) design shows a clear trend toward integration of multiple processor cores on a single chip. Designing a multiprocessor system-on-chip (MPSOC) requires an understanding of the various design styles and techniques used in the multiprocessor. Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions. Multiprocessor Systems-on-Chips covers both design techniques and applications for MPSOCs. Design topics include multiprocessor architectures, processors, operating systems, compilers, methodologies, and synthesis algorithms, and application areas covered include telecommunications and multimedia. The majority of the chapters were collected from presentations made at the International Workshop on Application-Specific Multi-Processor SoC held over the past two years. The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs. After having refined their material at the workshop, the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology. *Examines several different architectures and the constraints imposed on them *Discusses scheduling, real-time operating systems, and compilers *Analyzes design trade-off and decisions in telecommunications and multimedia applications

ASIC/SoC Functional Design Verification Dec 07 2020 This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

Advanced HDL Synthesis and SOC Prototyping Apr 11 2021 This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

Co-verification of Hardware and Software for ARM SoC Design Jun 25 2022 Hardware/software co-verification is how to make sure that embedded system software works correctly with the hardware, and that the hardware has been properly designed to run the software successfully -before large sums are spent on prototypes or manufacturing. This is the first book to apply this verification technique to the rapidly growing field of embedded systems-on-a-chip(SoC). As traditional embedded system design evolves into single-chip design, embedded engineers must be armed with the necessary information to make educated decisions about which tools and methodology to deploy. SoC verification requires a mix of expertise from the disciplines of microprocessor and computer architecture, logic design and simulation, and C and Assembly language embedded software. Until now, the relevant information on how it all fits together has not been available. Andrews, a recognized expert, provides in-depth information about how co-verification really works, how to be successful using it, and pitfalls to avoid. He illustrates these concepts using concrete examples with the ARM core - a technology that has the dominant market share in embedded system product design. The companion CD-ROM contains all source code used in the design examples, a searchable e-book version, and useful design tools. * The only book on verification for systems-on-a-chip (SoC) on the market * Will save engineers and their companies time and money by showing them how to speed up the testing process, while still avoiding costly mistakes * Design examples use the ARM core, the dominant technology in SoC, and all the source code is included on the accompanying CD-Rom, so engineers can easily use it in their own designs

Hardware Software Co-Design of a Multimedia SOC Platform Jan 08 2021 Hardware Software Co-Design of a Multimedia SOC Platform is one of the first of its kinds to provide a comprehensive overview of the design and implementation of the hardware and software of an SoC platform for multimedia applications. Topics covered in this book range from system level design methodology, multimedia algorithm implementation, a sub-word parallel, single-instruction-multiple data (SIMD) processor design, and its virtual platform implementation, to the development of an SIMD parallel compiler as well as a real-time operating system (RTOS). Hardware Software Co-Design of a Multimedia SOC Platform is written for practitioner engineers and technical managers who want to gain first hand knowledge about the hardware-software design process of an SoC platform. It offers both tutorial-like details to help readers become familiar with a diverse range of subjects, and in-depth analysis for advanced readers to pursue further.

Software Architect’s Handbook Feb 09 2021 A comprehensive guide to exploring software architecture concepts and implementing best practices Key Features Enhance your skills to grow your career as a software architect Design efficient software architectures using patterns and best practices Learn how software architecture relates to an organization as well as software development methodology Book Description The Software Architect’s Handbook is a comprehensive guide to help developers, architects, and senior programmers advance their career in the software architecture domain. This book takes you through all the important concepts, right from design principles to different considerations at various stages of your career in software architecture. The book begins by covering the fundamentals, benefits, and purpose of software architecture. You will discover how software architecture relates to an organization, followed by identifying its significant quality attributes. Once you have covered the basics, you will

explore design patterns, best practices, and paradigms for efficient software development. The book discusses which factors you need to consider for performance and security enhancements. You will learn to write documentation for your architectures and make appropriate decisions when considering DevOps. In addition to this, you will explore how to design legacy applications before understanding how to create software architectures that evolve as the market, business requirements, frameworks, tools, and best practices change over time. By the end of this book, you will not only have studied software architecture concepts but also built the soft skills necessary to grow in this field. What you will learn Design software architectures using patterns and best practices Explore the different considerations for designing software architecture Discover what it takes to continuously improve as a software architect Create loosely coupled systems that can support change Understand DevOps and how it affects software architecture Integrate, refactor, and re-architect legacy applications Who this book is for The Software Architect's Handbook is for you if you are a software architect, chief technical officer (CTO), or senior developer looking to gain a firm grasp of software architecture.

On-Chip Communication Architectures Jul 14 2021 Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years

A Practical Approach to VLSI System on Chip (SoC) Design Aug 27 2022 This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

Embedded System Design Apr 30 2020 The book's aim is to highlight all the complex issues, tasks and techniques that must be mastered by a SoC Architect to define and architect SoC for an embedded application. This book is primary focused on real problems with emphasis on architectural techniques across various aspects of chip-design, especially in context to embedded systems. The book covers aspects of embedded systems in a consistent way, starting with basic concepts that provides introduction to embedded systems and gradually increasing the depth to reach advanced concepts, such as power management and design consideration for maximum power efficiency and higher battery life. Theoretical part has been intentionally kept to the minimum that is essentially required to understand the subject. The guidelines explained across various chapters are independent of any CAD tool or silicon process and are applicable to any SoC architecture targeted for embedded systems.

Interconnect-Centric Design for Advanced SOC and NOC Nov 18 2021 In Interconnect-centric Design for Advanced SoC and NoC, we have tried to create a comprehensive understanding about on-chip interconnect characteristics, design methodologies, layered views on different abstraction levels and finally about applying the interconnect-centric design in system-on-chip design. Traditionally, on-chip communication design has been done using rather ad-hoc and informal approaches that fail to meet some of the challenges posed by next-generation SOC designs, such as performance and throughput, power and energy, reliability, predictability, synchronization, and management of concurrency. To address these challenges, it is critical to take a global view of the communication problem, and decompose it along lines that make it more tractable. We believe that a layered approach similar to that defined by the communication networks community should also be used for on-chip communication design. The design issues are handled on physical and circuit layer, logic and architecture layer, and from system design methodology and tools point of view. Formal communication modeling and refinement is used to bridge the communication layers, and network-centric modeling of multiprocessor on-chip networks and socket-based design will serve the development of platforms for SoC and NoC integration. Interconnect-centric Design for Advanced SoC and NoC is concluded by two application examples: interconnect and memory organization in SoCs for advanced set-top boxes and TV, and a case study in NoC platform design for more generic applications.

Low-Power NoC for High-Performance SoC Design Oct 17 2021 Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling Language (UML) throughout, it presents complicated concepts, such as models of computation and communication–computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

Essential Issues in SOC Design Jul 26 2022 This book originated from a workshop held at the DATE 2005 conference, namely Designing Complex SOCs. State-of-the-art in issues related to System-on-Chip (SoC) design by leading experts in the fields, it covers IP development, verification, integration, chip implementation, testing and software. It contains valuable academic and industrial examples for those involved with the design of complex SOCs.

Computer System Design Mar 22 2022 The next generation of computer system designers will be less concerned about details of processors and memories, and more concerned about the elements of a system tailored to particular applications. These designers will have a fundamental knowledge of processors and other elements in the system, but the success of their design will depend on the skills in making system-level tradeoffs that optimize the cost, performance and other attributes to meet application requirements. This book provides a new treatment of computer system design, particularly for System-on-Chip (SOC), which addresses the issues mentioned above. It begins with a global introduction, from the high-level view to the lowest common denominator (the chip itself), then moves on to the three main building blocks of an SOC (processor, memory, and interconnect). Next is an overview of what makes SOC unique (its customization ability and the applications that drive it). The final chapter presents future challenges for system design and SOC possibilities.

Arm System-On-Chip Architecture, 2/E Aug 23 2019

VLSI-Soc Oct 05 2020

System-on-a-Chip Verification Jan 28 2020 This is the first book to cover verification strategies and methodologies for SOC verification from

system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth application.
Fundamentals of IP and SoC Security Sep 04 2020 This book is about security in embedded systems and it provides an authoritative reference to all aspects of security in system-on-chip (SoC) designs. The authors discuss issues ranging from security requirements in SoC designs, definition of architectures and design choices to enforce and validate security policies, and trade-offs and conflicts involving security, functionality, and debug requirements. Coverage also includes case studies from the “trenches” of current industrial practice in design, implementation, and validation of security-critical embedded systems. Provides an authoritative reference and summary of the current state-of-the-art in security for embedded systems, hardware IPs and SoC designs; Takes a "cross-cutting" view of security that interacts with different design and validation components such as architecture, implementation, verification, and debug, each enforcing unique trade-offs; Includes high-level overview, detailed analysis on implementation, and relevant case studies on design/verification/debug issues related to IP/SoC security.
System-on-Chip Security Nov 25 2019 This book describes a wide variety of System-on-Chip (SoC) security threats and vulnerabilities, as well as their sources, in each stage of a design life cycle. The authors discuss a wide variety of state-of-the-art security verification and validation approaches such as formal methods and side-channel analysis, as well as simulation-based security and trust validation approaches. This book provides a comprehensive reference for system on chip designers and verification and validation engineers interested in verifying security and trust of heterogeneous SoCs.
VLSI-SoC: Design Methodologies for SoC and SiP Jul 02 2020 This book contains extended and revised versions of the best papers that were p- sented during the 16th edition of the IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration, a global System-on-a-Chip Design & CAD conference. The 16th conference was held at the Grand Hotel of Rhodes Island, Greece (October 13–15, 2008). Previous conferences have taken place in Edinburgh, Trondheim, V-couver, Munich, Grenoble, Tokyo, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice and Atlanta. VLSI-SoC 2008 was the 16th in a series of international conferences sponsored by IFIP TC 10 Working Group 10.5 and IEEE CEDA that explores the state of the art and the new developments in the field of VLSI systems and their designs. The purpose of the conference was to provide a forum to exchange ideas and to present industrial and research results in the fields of VLSI/ULSI systems, embedded systems and - croelectronic design and test.
System-on-Chip Design with Arm® Cortex®-M Processors Feb 21 2022 The Arm(R) Cortex(R)-M processors are already one of the most popular choices for loT and embedded applications. With Arm Flexible Access and DesignStart(TM), accessing Arm Cortex-M processor IP is fast, affordable, and easy. This book introduces all the key topics that system-on-chip (SoC) and FPGA designers need to know when integrating a Cortex-M processor into their design, including bus protocols, bus interconnect, and peripheral designs. Joseph Yiu is a distinguished Arm engineer who began designing SoCs back in 2000 and has been a leader in this field for nearly twenty years. Joseph's book takes an expert look at what SoC designers need to know when incorporating Cortex-M processors into their systems. He discusses the on-chip bus protocol specifications (AMBA, AHB, and APB), used by Arm processors and a wide range of on-chip digital components such as memory interfaces, peripherals, and debug components. Software development and advanced design considerations are also covered. The journey concludes with 'Putting the system together', a designer's eye view of a simple microcontroller-like design based on the Cortex-M3 processor (DesignStart) that uses the components that you will have learned to create.
The Simple Art of SoC Design Apr 23 2022 This book tackles head-on the challenges of digital design in the era of billion-transistor SoCs. It discusses fundamental design concepts in design and coding required to produce robust, functionally correct designs. It also provides specific techniques for measuring and minimizing complexity in RTL code. Finally, it discusses the tradeoff between RTL and high-level (C-based) design and how tools and languages must progress to address the needs of tomorrow’s SoC designs.
System-on-a-chip Mar 30 2020 Starting with a basic overview of system-on-a-chip (SoC), including definitions of related terms, this new book helps you understand SoC design challenges, and the latest design and test methodologies. You see how ASIC technology evolved to an embedded cores-based concept that includes pre-designed, reusable Intellectual Property (IP) cores that act as microprocessors, data storage devices, DSP, bus control, and interfaces -- all "stitched" together by a User's Defined Logic (UDL).
System on Chip Interfaces for Low Power Design Dec 19 2021 System on Chip Interfaces for Low Power Design provides a top-down understanding of interfaces available to SoC developers, not only the underlying protocols and architecture of each, but also how they interact and the tradeoffs involved. The book offers a common context to help understand the variety of available interfaces and make sense of technology from different vendors aligned with multiple standards. With particular emphasis on power as a factor, the authors explain how each interface performs in various usage scenarios and discuss their advantages and disadvantages. Readers learn to make educated decisions on what interfaces to use when designing systems and gain insight for innovating new/custom interfaces for a subsystem and their potential impact. Provides a top-down guide to SoC interfaces for memory, multimedia, sensors, display, and communication Explores the underlying protocols and architecture of each interface with multiple examples Guides through competing standards and explains how different interfaces might interact or interfere with each other Explains challenges in system design, validation, debugging and their impact on development